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An Integrated Method for Transistor-to-Gate Level Performance Degradation Analysis

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Abstract: *In this research, an integrated method to analyse the degradation of performance in digital circuit is brought out through the transistor level to the gate level. To accurately predict circuit behaviour with time, by incorporating both gate-level analysis of timing with device-level ageing models the proposed methodology provides a framework to achieve this. The method also includes process variation, bias temperature instability (BTI) and hot carrier injection (HCI) effects to enable comprehensive deterioration monitoring over base cell libraries. The combination of gate-level timing models and SPICE-level degradation data can be used to efficiently and correctly identify the aging-related design issues by using the hybrid-simulation-based design evaluation. Experiments on benchmark circuits yield improvement in the accuracy of the forecast, as well as aging-prone key paths. This approach is enhanced in sophisticated semiconductor technology to ensure design optimisation that ensures long term reliability.*

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I. Introduction

The ageing effects that cause performance degradation of a semiconductor device has become a key concern in the ability to produce reliable circuit designs as the semiconductor technology progresses to deep submicron and nanometre dimensions. Ageing Mechanisms important to gate-level functionality and overall circuit performance are of primary importance since Hot Carrier Injection (HCI) and Bias Temperature Instability (BTI) are well-known causes of transistor performance drift in time. The limit to accuracy and scalability is the default of the traditional analytic tools of treating the device-level and gate-level degradation separately.

To propose a unified approach to offer a coherent paradigm to forecast degradation in performance, this study recommends a complete technique that associates transistor-level but also transistor-level research with gate degree analysis. The proposed technique allows considering critical temporal paths early in order to better optimize reliability-aware design and also link low-level physical influences with high-level design measures. Such validation of the proposed methodology is done by the implementation of standard benchmark circuits that demonstrate higher precision in identification of timing violations due to ageing and that will serve as useful information on long-termed performance behaviour on different technology nodes.

II. Simulation Tool

Simulation tool under this methodology simulates the effects of ageing such as BTI and HCI by providing the capability to analyze transistor level as well as gate level effect. SPICE-level simulation of circuit is used to accurately characterise degrading behaviours of devices with time. These results are then abstracted to timing models that are usable by global EDA gate-level tools such as Cadence Tempus or Synopsys Prime Time to evaluate performance impact through regular cells. It is a hybrid flow: it relies upon timing characterisation scripts to move delay degradation information results of aging-aware SPICE simulations into gate-level netlists. The process is automated by means of Custom TCL or Python scripts so that the data flow between gate-level timing engine and SPICE simulator was easy.

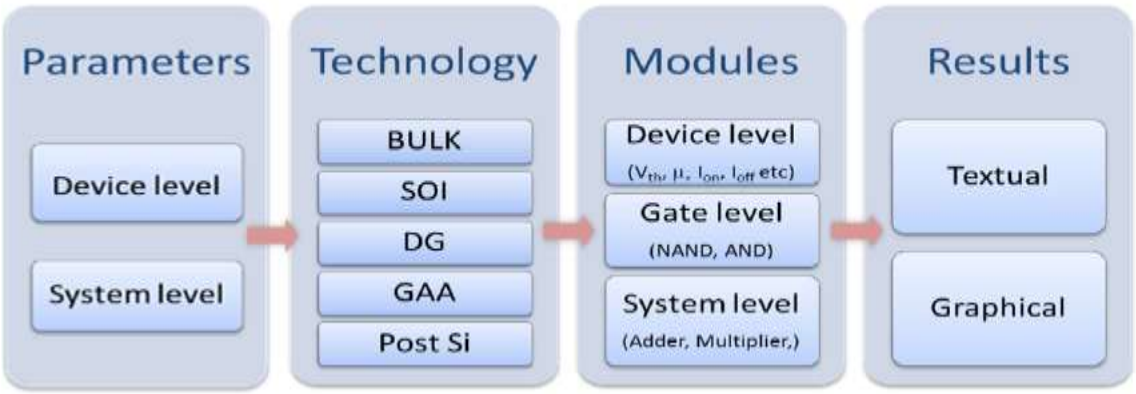

Fig 1: TAMTAMS analysis flow

A balance between accuracy and computing expense is crossed making it possible to study large circuits within an acceptable time thus it is suitable with the long-term analysis of performance and reliability at an industrial magnitude.

III. Transistor Performance Degradation

Extended degradation of the electrical characteristics of a transistor over time, largely caused by such ageing mechanisms as Time-Dependent Dielectric Breakdown (TDDB) and Hot Carrier Injection (HCI) and Bias Temperature Instability (BTI), is known as transistor performance degradation. With change in threshold voltage, BTI- Positive BTI (PBTI) in the case of NMOS and Negative BTI (NBTI) in the case of PMOS- causes latency increase and current drive current reduction. The gate oxide contact is damaged by high-energy carriers that end up in the reduction of carrier mobility and greater delay degradation being the main cause of HCI. The amplification of electric fields, and the limit in scaling down in deep submicron and FinFET technologies makes it even more serious.

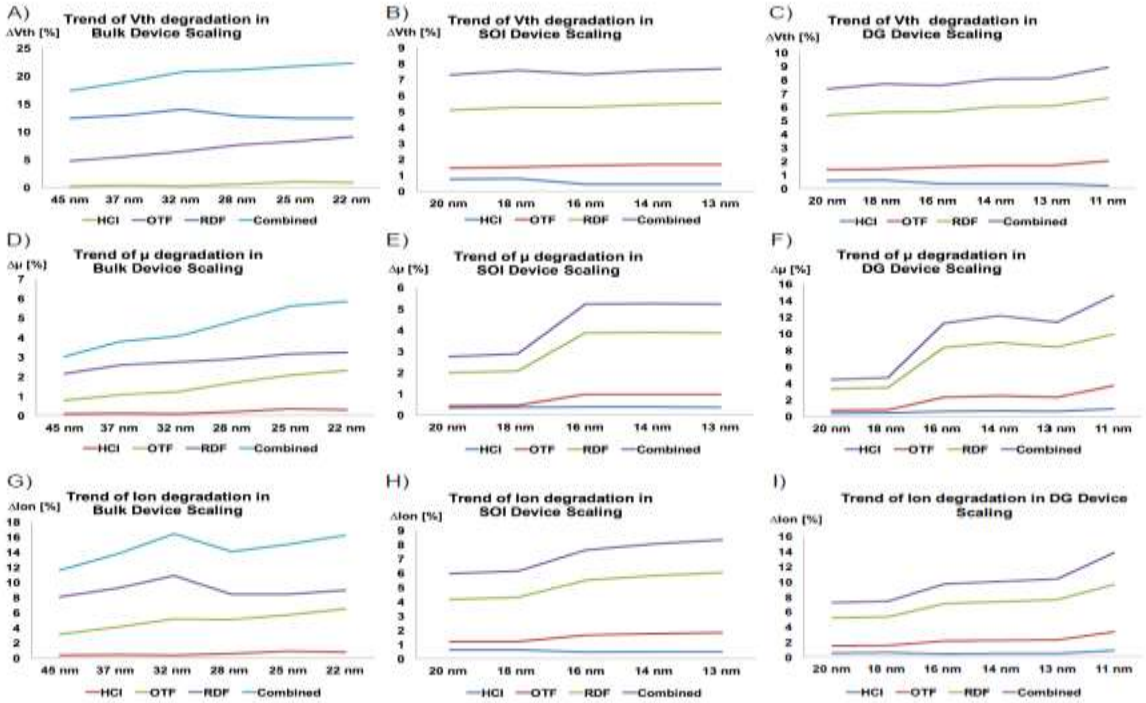

Fig 2: Trend of Vth and Ion

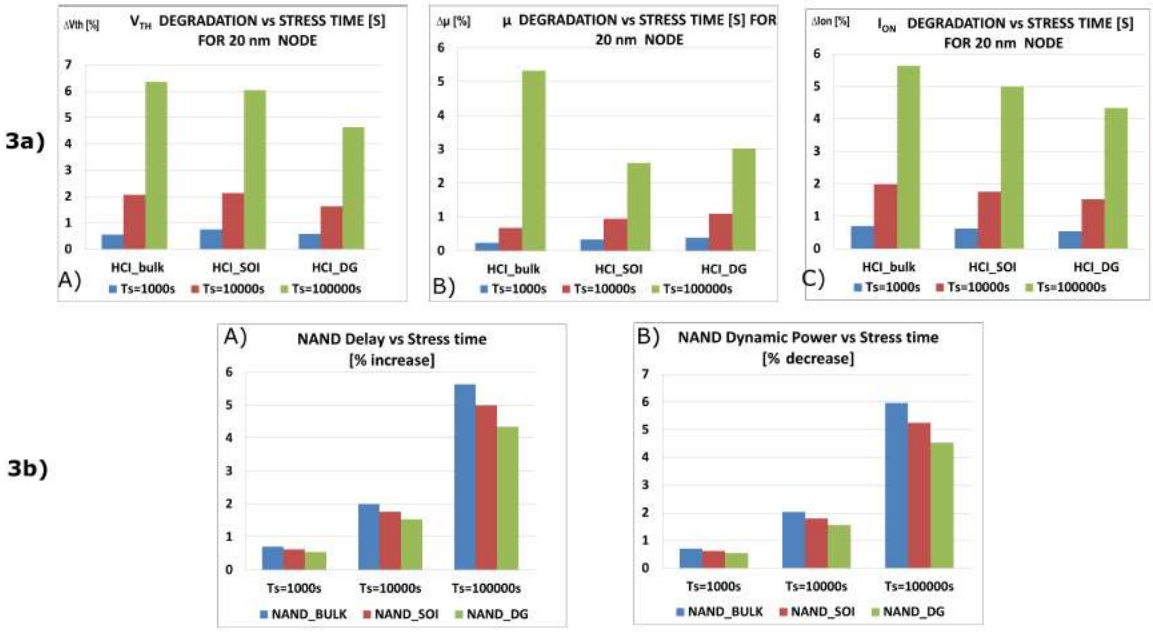

Fig 3: HCI induced performance degradation

Logic gates latency increases due to accumulated degraded and overloads the critical routes exceeding the timing margins leading to functional failures. Ageing impact modelling and the assurance of circuit reliability requires accurate transistor-level modelling. The simulation technology is the guiding tool of age-aware design solutions that gives the long-term effects on performance based on stress and recovery models.

IV. Conclusion

To help meet the increasing reliability issues in the future semiconductor technologies, the study in question shall present a simplified approach toward analyzing the degraded performance at transistor level to gate level. Combined with gate-level timing analysis and large transistor-level models of the ageing effect, the proposed approach offers a complete and accurate approach at predicting the ageing issue of a circuit with time. The consideration of the significant ageing factors as BTI and HCI will allow a realistic modelling of time-dependent changes of delay. Because the hybrid simulation method embraces the successful gap closure between the gate-level performance analysis and even the degradation data at the SPICE level, it is able to detect important route violations in the initial stages as well as elevate the proactive design optimisation. The accuracy and scalability of the method of detailed designs is verified experimentally over benchmark circuits. This combination analysis methodology helps in designing robust and age-resistant digital systems because it would provide valuable insight into the behaviour of circuits over a long period. The present study is a potential area of interest to be dealt with in the future, whereby the method can be focussed into the inclusion of adaptive ageing mitigation strategies as well as the new technology.

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